BlueSoleil i50e-A Datasheet

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Version 1.0

VERSION HISTORY

REVISION	AMENDMENT	DATE	AUTHOR
1.0	Initial version	2014-2-21	Wan Zhifu Li Li

Contents

BlueSoleil i50e-A

DESCRIPTION

BlueSoleil i50e-A is a *Bluetooth* 3.0 +EDR (Enhanced Data Rates) class 2module. It contains all the necessary elements from *Bluetooth* radio to antenna and a fully implemented protocol stack.

By default i50e-A module is equipped with powerful and easy-to-use BlueSoleil firmware. BlueSoleil enables users to access *Bluetooth* functionality with simple ASCII commands delivered to the module over serial interface - it's just like a *Bluetooth* modem.

Therefore, i50e-A provides an ideal solution for developers who want to integrate *Bluetooth* wireless technology into their design.

FEATURES

- Fully Qualified *Bluetooth* system v3.0+ EDR
- BQB, KCC, TELEC Certification
- Industrial temperature range from -40^{0}C to +85^{0}C
- Integrated audio codec, acoustic echo cancellation algorithm
- Support for 802.11 Coexistence
- 8Mbits or 16Mbits of Flash Memory
- Low power consumption
- RoHS Compliant

APPLICATIONS

- High quality stereo headsets
- High quality mono headsets
- Hands-free car kits
- Wireless speakers
- IVI *Bluetooth* Solution

Figure 1 BlueSoleil i50e

1 Block Diagram and Descriptions

BlueSoleil i50e-A's block diagram is illustrated in Figure 2 below.

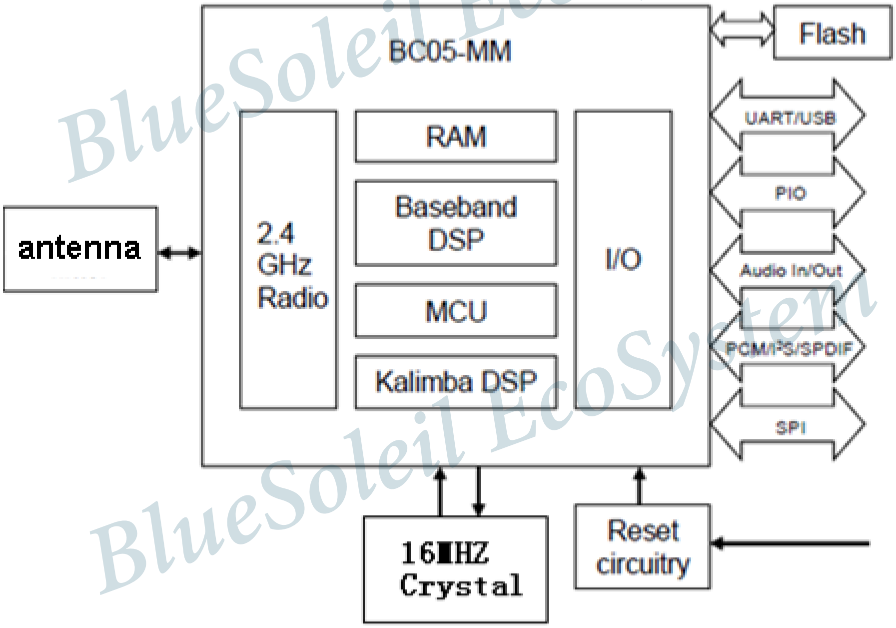

Figure 2 i50e-A Block Diagram

BC05-MM

The BlueCore05-MM is a single-chip radio and baseband IC for *Bluetooth* 2.4GHz systems. It provides a fully compliant *Bluetooth* system to v3.0+EDR of the specification for data and voice. BlueCore05-MM contains the Kalimba DSP co-processor with double the MIPS of BlueCore03-MM, supporting enhanced audio applications. BlueCore05-MM integrates a 16-bit stereo codec and it has a fully differential audio interface with a low noise microphone bias.

Crystal

The crystal oscillates at 16MHz.

Flash

Flash memory is used for storing the *Bluetooth* protocol stack and Virtual Machine applications. It can also be used as an optional external RAM for memory-intensive applications.

Balanced Filter

Combined balun and filter changes the balanced input/output signal of the module to unbalanced signal of the antenna. The filter is a band pass filter (ISM band).

USB

The USB interface is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. i50e-A acts as a USB peripheral, responding to requests from a Master host controller such as a Personal Computer (PC).

Synchronous Serial Interface

This interface is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for i50e-A debugging. It can also be used for programming the Flash memory.

UART

This interface is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices. UART is usually used to operate i50e-A by ASCII commands from MCU.

PCM / I2S / SPDIF Interface

This interface is a bi-directional serial programmable audio interface supporting PCM, I2S and SPDIF formats.

Audio Interface

The audio interface of i50e-A has fully differential inputs and outputs and a microphone bias output. A high-quality stereo audio *Bluetooth* application can be implemented with minimum amount of external components.

Programmable I/O

i50e-A has a total of 14 digital programmable I/O terminals. These are controlled by the firmware running on the device.

Reset

I50e-A has a reset circuitry that is used to reset the module in the startup to ensure proper operation of the flash memory. Alternatively, the reset can be externally driven by using a i50e-A reset pin.

2 Electrical Characteristics

2.1 Absolute maximum ratings

The module should not continuously run under extreme conditions. The absolute maximum ratings are summarized in Table 1 below. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

Table 1 Absolute Maximum Ratings

	Min	Max	Unit
Storage temperature	-40	85	°C
Operating temperature	-40	85	°C
Supply voltage	-0.3	3.6	V
Terminal voltages	Vss-0.4	Vdd + 0.4	V

2.2 Recommended Operating Conditions

Recommended operating conditions are summarized in Table 2 below.

Table 2 Recommended Operating Conditions

	Min	Typ	Max	Unit
Operating temperature	-30	20	85	°C
VDD_IO	1.7	3.3	3.6	V
VDD_BAT	2.5	3.3	4.4	V
VDD_CHG	0	3.3	6.5	V
Terminal voltages	0		Vdd	V

2.3 Terminal characteristics

BlueSoleil i50e-A's terminal characteristics are summarized in Table 3 below.

Table 3 Terminal Characteristics

	Min	Typ	Max	Unit
I/O voltage levels				
VIL input logic level low	-0.4	-	0.8	V
VIH input logic level high	0.7×Vdd	-	Vdd + 0.4	V
VOL output logic level low	-	-	0.2	V
VOH output logic level high	0.75×Vdd	-	VDD	V
Reset terminal				
VTH,res threshold voltage	0.64	0.85	1.5	V

RIRES input resistance		220		kΩ
CIRES input capacitance		220		nF
Input and tri-state current with				
Strong pull-up	-100	-40	-10	µA
Strong pull-down	10	40	100	µA
Weak pull-up	-5	-1	-0,2	µA
Weak pull-down	0,2	1	5	µA
I/O pad leakage current	-1	0	1	µA
LED driver pad				
Off current	-	1	2	µA
On resistance(V_{pad})	-	20	33	Ω
On resistance, pad enabled by battery charger(V_{pad}< 0.5V)	-	20	50	Ω

2.4Battery charger

BlueSoleil i50e-A's battery charger characteristics are summarized in Table 4 below.

Table 4 Battery Charger Characteristic

		Min	Typ.	Max	Unit
VDD_CHG	-	4.5	-	6.5	V
Supply current (a)		-	4.5	6	mA
Battery trickle charge current (b) (c)	Maximum setting	-	14	-	mA
	Minimum setting	-	4	-	mA
Maximum battery fast charge current (d) (c)	Headroom > 0.7 V (e)	-	140	-	mA
HeadrooTHD+N 16Ω load		-		0.1	%
m = 0.3 V		-	120	-	mA
Minimum battery fast charge current (d) (c)	Headroom > 0.7 V	-	40	-	mA
	Headroom = 0.3 V	-	35	-	mA
Trickle charge voltage threshold		-	2.9	-	V
Float voltage (with correct trim value set), VFLOAT(f)		4.17	4.2	4.23	V
Float voltage trim step size (f)		-	50	-	mV
Battery charge termination current, as a percentage of the fast charge current		5	10	20	%
Supply current (a)		-	1.5	2	mA
Battery current		-	-5	-	µA
Battery recharge hysteresis (g)		100	-	200	mV
VDD_CHG under-voltage threshold	VDD_CHG rising	-	3.9	-	V
	VDD_CHG falling	-	3.7	-	V
VDD_CHG - BAT_P lockout	VDD_CHG rising	-	0.22	-	V

threshold	VDD_CHG falling	-	0.17	-	V
Supply current		-	1.5	2	mA
Battery current		-1	-	0	µA

(a) Current into VDD_CHG - does not include current delivered to battery (I VDD_CHG - I BAT_P)

(b) BAT_P < Float voltage

(c) Charge current can be set in 16 equally spaced steps

(d) Trickle charge threshold < BAT_P < Float voltage

(e) Where headroom = VDD_CHG - BAT_P

(f) Float voltage can be adjusted in 15 steps. Trim setting is determined in production test and must be loaded into the battery charger by firmware during boot-up sequence

(g) Hysteresis of (VFLOAT - BAT_P) for charging to restart

2.5 CODEC Characteristics

BlueSoleil i50e-A's battery charger characteristics are summarized in Table 5 and Table 6 below.

Table 5 Stereo CODEC ADC Characteristics

Parameter	Conditions		Min	Typ	Max	Unit
Resolution			-	-	16	Bits
Input Sample Rate, Fsample			8	-	48	kHz
Signal to Noise Ratio, SNR	fin = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 1% 150mVpk-pk input	Fsample	-	-	-	-
		8 kHz	-	95	-	dB
		11.025 kHz	-	95	-	dB
		16 kHz	-	95	-	dB
		22.050 kHz	-	95	-	dB
		32 kHz	-	95	-	dB
		44.1 kHz	-	95	-	dB
Digital Gain	Digital Gain Resolution = 1/32dB		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		0	-	-21	dB
Output voltage full scale swing (differential)			-	750	-	mV rms
Allowed Load ResistiveCapacitive			16(8)	-	OC	Ω
			-	-	500	pF
THD+N 100kΩ load			-	-	0.01	%
SNR (Load = 16Ω, 0dBFS input relative to digital silence)			-	95	-	dB
Stereo CODEC Digital to Analog Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution			-	-	16	Bits
Input Sample Rate, Fsample			8	-	48	kHz

Table 6 Stereo CODEC DAC Characteristics

Parameters	Conditions		Min	Typ	Max	Unit
Resolution			-	-	16	Bits
Input Sample Rate, Fsample			8	-	44.1	kHz
Signal to Noise Ratio, SNR	fin = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 1% 150mVpk-pk input	Fsample	-	-	-	-
		8 kHz	-	82	-	dB
		11.025 kHz	-	81	-	dB
		16 kHz	-	80	-	dB
		22.050 kHz	-	79	-	dB
		32 kHz	-	79	-	dB
		44.1 kHz	-	78	-	dB
Digital Gain	Digital Gain Resolution = 1/32dB		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		-3	-	42	dB
Input full scale at maximum gain (differential)			-	4	-	mV rms
Input full scale at minimum gain (differential)			-	800	-	mV rms
3dB Bandwidth			-	20	-	kHz
Microphone mode input impedance			-	6.0	-	kΩ
THD+N (microphone input) @ 30mV rms input			-	0.04	-	%

2.6 Current Consumption

BlueSoleil i50's current consumption is summarized in Table 7 below.

Table 7 Current Consumption

Operation Mode	Connection Type	UART Rate (kbps)	Average	Unit
Inquiry and Page scan	-	-	4	mA
No data traffic after connecting mobile phone	-	9.6	4.2	mA
Stereo music traffic	Slave	9.6	30	mA
	Master	115.2	28	mA
(e)SCO traffic, that is, hands-free	Slave	9.6	34.7	mA
	Master	115.2	29	mA

2.7 Radio Characteristics and General Specifications

BlueSoleil i50's radio characteristics and general specifications are summarized in Table 8 below.

Table 8 Radio Characteristics and General Specifications

	Specification		Note
Operating frequency range	(2400 ... 2483,5) MHz		ISM Band
Lower quard band	2 MHz		
Upper quard band	3,5 MHz		
Carrier frequency	2402 MHz ... 2480 MHz		f = 2402 + k, k = 0...78
Modulation method	GFSK (1 Mbps) P/4 DQPSK (2Mbps)		
Hopping	1600 hops/s, 1 MHz channel space		
Maximum data rate	GFSK	Asynchronous, 723.2 kbps / 57.6 kbps Synchronous: 433.9 kbps / 433.9 kbps	
	P/4 DQPSK	Asynchronous, 1448.5 kbps / 115.2 kbps Synchronous: 869.7 kbps / 869.7 kbps	
	8DQPSK	Asynchronous, 2178.1 kbps / 177.2 kbps Synchronous: 1306.9 kbps / 1306.9 kbps	
Receiving signal range	-82 to -20 dBm		Typical condition
Receiver IF frequency	1.5 MHz		Center frequency
Transmission power	Min	-11 ... -9 dBm	
	Max	+1 ... +3 dBm	
RF input impedance	50		
Compliance	*Bluetooth* specification, version 2.0 + EDR		
USB specification	USB specification, version 1.1 (USB 2.0 compliant)		

3 Pin Description

BlueSoleil i50e-A's PIN description refers to Figure 3 and Table 9.

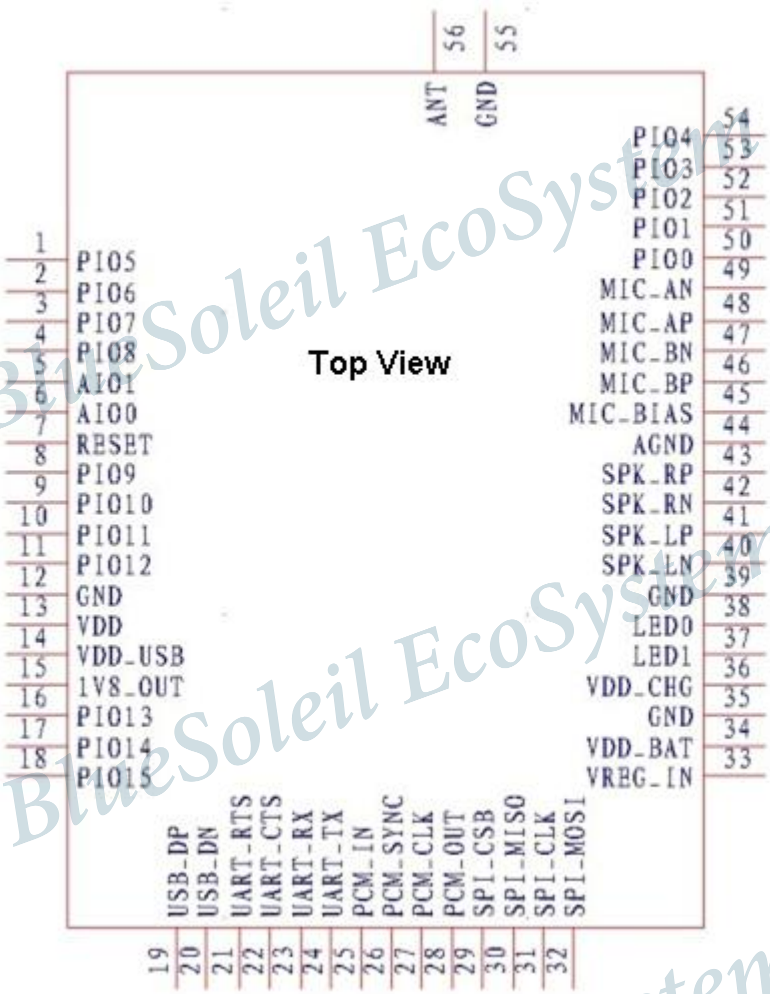

Figure 3 i50e-A PIN Diagram (Top View)

Table 9 PIN Definition

PIN NO.	Name	Type	Function
1	PIO5	Bi-directional	Programmable input/output line
2	PIO6	Bi-directional	Programmable input/output line
3	PIO7	Bi-directional	Programmable input/output line
4	PIO8	Bi-directional	Programmable input/output line
5	AIO1	Bi-directional	Programmable input/output line

6	AIO0	Bi-directional	Programmable input/output line
7	RESET	CMOS Input with weak internal pull-up	Reset if low. Input debounced so must be 5ms to cause a reset
8	PIO9	Bi-directional	Programmable input/output line
9	PIO10	Bi-directional	Programmable input/output line
10	PIO11	Bi-directional	Programmable input/output line
11	PIO12	Bi-directional	Programmable input/output line
12	GND	GND	Ground
13	VDD	Power	+3.3V power supply
14	VDD_USB	Power	Positive supply for UART/USB ports
15	VDD_1.8V_OUT	Power	+1.8V power output
16	PIO13	Bi-directional	Programmable input/output line
17	PIO14	Bi-directional	Programmable input/output line
18	PIO15	Bi-directional	Programmable input/output line
19	USB_DP	Bi-directional	USB Date plus
20	USB_DN	Bi-directional	USB Date minus
21	UART_RTS	CMOS Output	UART Request to Send (active low)
22	UART_CTS	CMOS Input	UART Clear to Send (active low)
23	UART_RX	CMOS Input	UART Data input
24	UART_TX	CMOS Output	UART Data output
25	PCM_IN	CMOS Input	Synchronous data input
26	PCM_SYNC	Bi-directional	Synchronous data Sync

27	PCM_CLK	Bi-directional	Synchronous data clock
28	PCM_OUT	CMOS Output	Synchronous data output
29	NC		Used for manufactory
30	NC		Used for manufactory
31	NC		Used for manufactory
32	NC		Used for manufactory
33	VREG_IN	analogue	Take high to enable
34	VDD_BAT	Battery terminal	Lithium ion/polymer battery positive terminal. Battery charger output and input to switch- mode regulator
35	GND	GND	Ground
36	VDD_CHG	Charger input	Lithium ion/polymer battery charger input
37	LED1	Open drain output	LED driver
38	LED0	Open drain output	LED driver
39	GND	GND	Ground
40	SPK_L_N	Analogue	Speaker output negative , left
41	SPK_L_P	Analogue	Speaker output positive , left
42	SPK_R_N	Analogue	Speaker output negative , right
43	SPK_R_P	Analogue	Speaker output positive , right
44	GND	GND	Ground
45	MIC_BIAS	Analogue	Microphone bias
46	MIC_B_P	Analogue	Microphone input positive , right

47	MIC_B_N	Analogue	Microphone input negative , right
48	MIC_A_P	Analogue	Microphone input positive , left
49	MIC_A_N	Analogue	Microphone input negative , left
50	PIO0	Bi-directional	Programmable input/output line
51	PIO1	Bi-directional	Programmable input/output line
52	PIO2	Bi-directional	Programmable input/output line
53	PIO3	Bi-directional	Programmable input/output line
54	PIO4	Bi-directional	Programmable input/output line
55	GND	GND	Ground
56	ANT	RF Interface	External antenna

VDD_IO

Supply voltage connection for the digital I/Os of the module. Supply voltage at this pin can vary between 1.8 V and 3.3 V. Output voltage swing at the digital terminals of i50e-A is 0 to VDD_IO.

VDD_USB

Positive supply for UART/USB ports.

VDD_BAT

Input for an internal 1.8 V switched mode regulator combined with output of the internal battery charger. See chapter 4.2 for detailed description for the charger. When not powered from a battery, VDD_IO and VDD_BAT can be combined to a single 3.3 V supply voltage.

VRE_IN

Enable pin for the internal 1,8 V regulator. This pin should be combined to a 3.3V supply voltage.

VDD_CHG

Charger input voltage. The charger will start operating when voltage to this pin is applied. When the charger is not used, this pin should be left floating. See chapter 4.2 for detailed description of the charger.

RESET

The RESET pin is an active low reset. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

PIO0 – PIO15

Programmable digital I/O lines. All PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. Configuration for each PIO line depends on the application. Default configuration for unused PIO lines is low.

AIO0 – AIO1

AIOs can be used to monitor analogue voltages such as a temperature sensor for the battery charger. AIOs can also be configured to be used as digital I/Os. The voltage level at these pins is 0 V to 1.5 V.

UART_RTS

CMOS output with weak internal pull-up. Can be used to implement RS232 hardware flow control where RTS (request to send) is active low indicator. UART interface requires external RS232 transceiver chip.

UART_CTS

CMOS input with weak internal pull-down. Can be used to implement RS232 hardware flow control where CTS (clear to send) is active low indicator. UART interface requires external RS232 transceiver chip.

UART_RXD

CMOS input with weak internal pull-down. UART_RXD is used to implement UART data transfer from another device to i50e-A. UART interface requires external RS232 transceiver chip.

UART_TXD

CMOS output with weak internal pull-up. TXD is used to implement UART data transfer from i50e-A to another device. UART interface requires external RS232 transceiver chip.

PCM_OUT

CMOS output with weak internal pull-down. Used in PCM (pulse code modulation) interface to transmit digitized audio. The PCM interface is shared with the I2S interface.

PCM_IN

CMOS input with weak internal pull-down. Used in PCM interface to receive digitized audio. The PCM interface is shared with the I2S interface.

PCM_CLK

Bi-directional synchronous data clock signal pin with weak internal pull-down. PCM_CLK is used in PCM interface to transmit or receive CLK signal. When configured as a master, i50e-A generates clock signal for the PCM interface. When configured as a slave PCM_CLK is an input and receives the clock signal from another device.

PCM_SYNC

A bi-directional synchronous data strobe with weak internal pull-down. When configured as a master, i50e-A generates SYNC signal for the PCM interface. When configured as a slave PCM_SYNC is an input and receives the SYNC signal from another device.

USB_D+

Bi-directional USB data line with a selectable internal 1.5 k pull-up implemented as a current source (compliant with USB specification v1.2) External series resistor is required to match the connection to the characteristic impedance of the USB cable.

USB_D-

Bi-directional USB data line. External series resistor is required to match the connection to the characteristic impedance of the USB cable.

MIC_B_N and MIC_B_P

Right channel audio inputs. This dual audio input can be configured to be either single-ended or fully differential and programmed for either microphone or line input. Route differential pairs close to each other and use a solid dedicated audio ground plane for the audio signals.

MIC_A_N and MIC_A_P

Left channel audio input. ESD protection and layout considerations similar to right channel audio should be used.

SPK_B_N and SPK_B_P

Right channel audio output. The audio output lines should be routed differentially to either the speakers or to the output amplifier, depending on whether or not a single-ended signal is required. Use low impedance ground plane dedicated for the audio signals.

SPK_A_N and SPK_A_P

Left channel audio output. The same guidelines apply to this section as discussed previously.

MIC_BIAS

Bias voltage output for a microphone. Use the same layout guidelines as discussed previously with other audio signals.

LED0/1

I50e-A includes a pad dedicated to driving LED indicators. This terminal may be controlled by firmware and it can also be set by the battery charger. The terminal is an open-drain output, so the LED must be connected from a positive supply rail to the pad in series with a current limiting resistor. It is recommended that the LED pad is operated with a pad voltage below 0.5V. In this case, the pad can be thought of as a resistor, RON. The resistance together with the external series resistor will set the current, ILED, in the LED. Value for the external series resistance can be calculated from the Equation 1.

$$I_{LED} = \frac{VDD - V_F}{R_{LED} + R_{ON}}$$

Equation 1 LED Series Resistor

Where VF is the forward voltage drop of the LED, ILED is the forward current of the LED and RON is on resistance (typically 20 Ω) of the LED driver.

4 Power Management

4.1 Power Management Block

BlueSoleil i50e-A contains an internal battery charger and a switch mode regulator that is mainly used for internal blocks of the module. See Figure 4 below. The module can be powered from a single 3.3 V supply provided that VDD_CHG is floating. Alternatively the module can be powered from a battery connected to VDD_BAT and using an external regulator for VDD_IO. 1.8 V to 3.3 V supply voltage for VDD_IO can be used to give desired signal levels for the digital interfaces of the module. USB, however, requires 3.3 V for proper operation and thus, when USB is in use, 3.3 V for VDD_IO is mandatory.AIO pins of the module use 1.8 V from the internal regulator and thus voltage level with these pins is within 0 V and 1.8 V.

VRE_IN is used to enable the on-chip regulator of i50e-A and should be taken high.

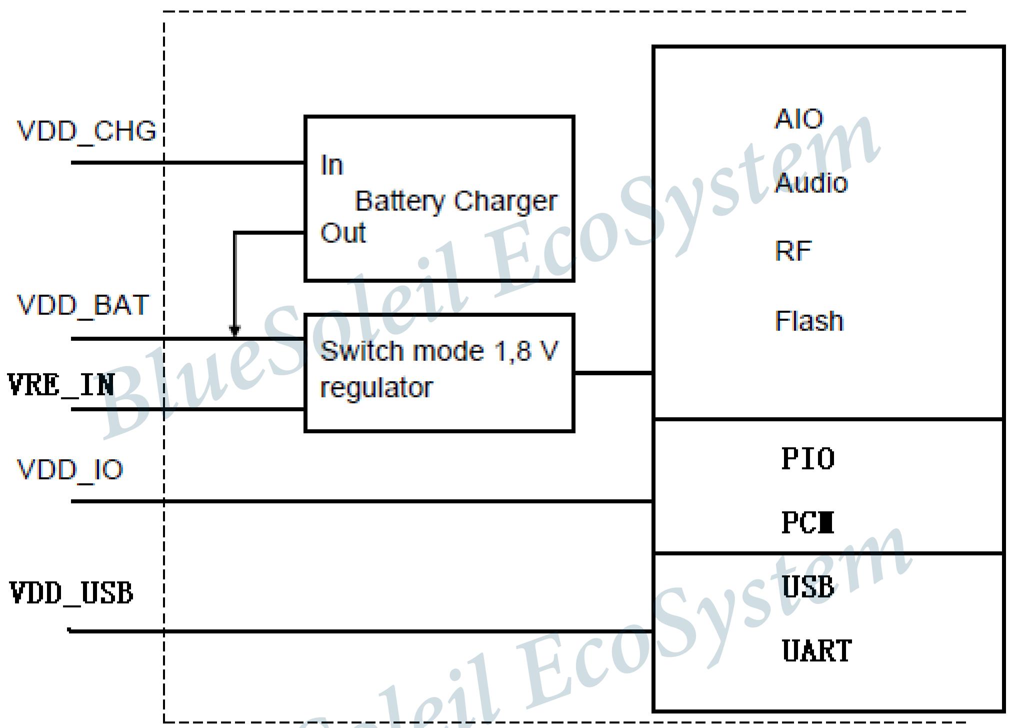

Figure 4 Power Management Block

4.2 Battery Charger

The battery charger is a constant current / constant voltage charger circuit, and is suitable for lithium ion/polymer batteries only. It shares a connection to the battery terminal, VDD_BAT, with the switch-mode regulator.

The constant current level can be varied to allow charging of different capacity batteries. I50e-A allows a number of different currents to be used in the battery charger hardware. Values written to PS key 0x039b CHARGER_CURRRENT in the range 1~15 specify the charger current from 40~135mA in even steps.Values outside the valid 0~15 range result in no change to the charging current. The default charging current (Key = 0) is nominally 40mA. Setting 0 is interpreted as "no-change" so will be ignored. The charger enters various states of operation as it charges a battery, including the following status:

- Off: entered when the charger is disconnected.
- Trickle Charge: entered when the battery voltage is below 2.9V.
- Fast Charge - Constant Current: entered when the battery voltage is above 2.9V.
- Fast Charge - Constant Voltage: entered when the battery has reached V_{float}, the charger switches mode to maintain the cell voltage at V_{float}voltage by adjusting the constant charge current.
- Standby: this is the state when the battery is fully charged and no charging takes place.

When a voltage is applied to the charger input terminal VDD_CHG, and the battery is not fully charged, the charger will operate and a LED connected to the terminal LED0 will illuminate. By default, until the firmware is running, the LED will pulse at a low-duty cycle to minimize current consumption. The battery charger circuitry auto-detects the presence of a power source, allowing the firmware to detect, using an internal status bit, when the charger is powered. Therefore, when the charger supply is not connected to VDD_CHG, the terminal must be left open circuit. The VDD_CHG pin, when not connected, must be allowed to float and not be pulled to a power rail. When the battery charger is not enabled, this pin may float to a low undefined voltage. Any DC connection will increase current consumption of the device. Capacitive components such as diodes, FETs, and ESD protection, may be connected. The battery charger is designed to operate with a permanently connected battery. If the application permits the charger input to be connected while the battery is disconnected, the VDD_BAT pin voltage may become unstable. This, in turn, may cause damage to the internal switch-mode regulator. Connecting a 470uF capacitor to VDD_BAT limits these oscillations thus preventing damage.

5 Serial Interfaces

5.1 UART Interface

BlueSoleil i50e-A Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices using the RS232 standard. See Figure 5 below. The UART interface of i50e-A uses voltage levels of 0 to Vdd and thus external transceiver IC is required to meet the voltage level specifications of UART.

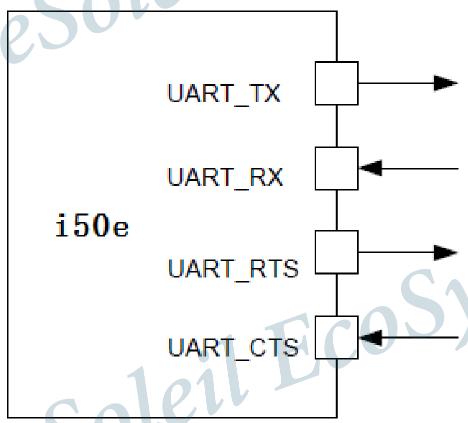

Figure 5 i50e-A UART interface

Table 10 Possible UART Settings

Parameters		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	3.0Mbaud (≤1%Error)
Flow control		RTS/CTS, none
Parity		None, Odd, Even
Number of stop bits		1 or 2
Bits per channel		8

Four signals are used to implement the UART function, as shown in Figure 5. When i50e-A is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. DTR, DSR and DCD signals can be implemented using PIO terminals of i50e-A. All UART connections are implemented using CMOS technology and have signaling levels of 0V and VDD. In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

The UART interface is capable of resetting i50e-A upon reception of a break signal. A Break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 6. If tBRK is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialize the system to a known state. Also, i50e-A can emit a Break character that may be used to wake the Host. See Figure 6 below.

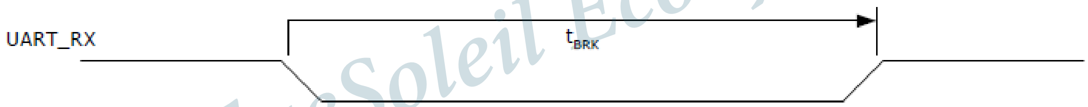

Figure 6 Break Signal

Since UART_RX terminal includes weak internal pull-down, it can’t be left open unless disabling UART interface using PS_KEY settings. If UART is not disabled, a pull-up resistor has to be connected to UART_RX. UART interface requires external RS232 transceiver, which usually includes the required pull-up.

Equation 2 shows a list of commonly used Baud rates and their associated values for the Persistent Store Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any Baud rate within the supported range can be set in the Persistent Store Key according to the formula in Equation 2 below.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUD\_RATE}}{0.004096}$$

Equation 2 Baud Rate Calculation Formula

Table 11 UART Baud Rates and Error Values

Baud Rate	Persistent store values		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	263	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2765800	0x2c3d	11325	0.00%

5.1.1 UART Configuration While RESET is Active

The UART interface for i50e-A while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when i50e-A reset is de-asserted and the firmware begins to run.

5.1.2 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on i50e-A can be used. The default state of i50e-A after reset is de-asserted, this is for the host UART bus to be connected to the i50e-A UART, thereby allowing communication to i50e-A via the UART.

In order to apply the UART bypass mode, a BCCMD command will be issued to i50e-A upon this, it will switch the bypass to PIO[7:4] as shown in Figure 7. Once the bypass mode has been invoked, i50e-A will enter the deep sleep state indefinitely.

In order to re-establish communication with i50e-A, the chip must be reset so that the default configuration takes affect.

It is important for the host to ensure a clean *Bluetooth* disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active *Bluetooth* links while operating the bypass mode.

The current consumption for a device in UART Bypass Mode is equal to the values quoted for a device in standby mode. See Figure 7 below.

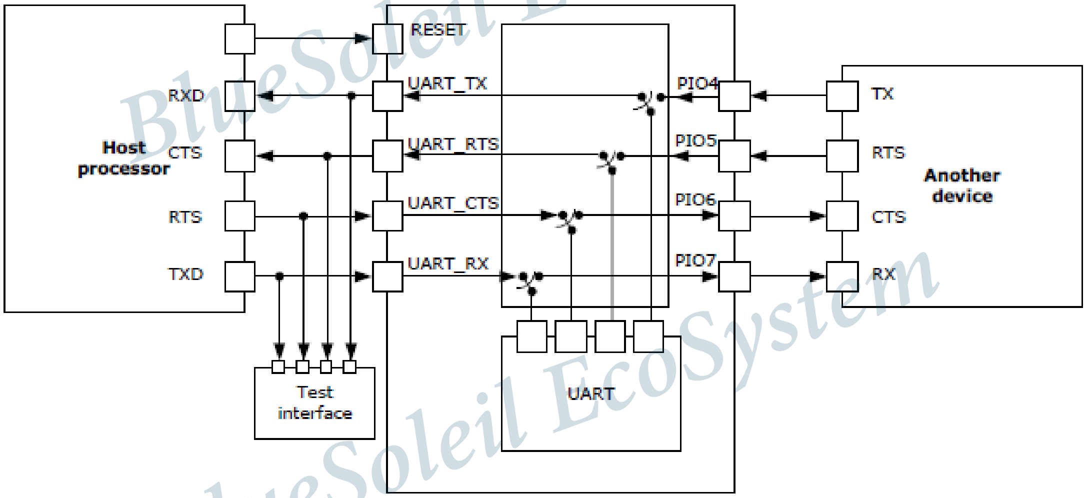

Figure 7 UART Bypass Mode

5.2 SPI Interface

The synchronous serial port interface (SPI) is for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory. SPI interface is connected using the MOSI, MISO, CSB and CLK pins. SPI interface is only used for debugging and updating firmware.

6 Audio Interfaces

6.1 Audio Interface

The audio interface circuit consists of the following components.

- Stereo audio CODEC
- Dual audio inputs and outputs

- A configurable PCM, I2S or SPDIF interface

Figure 8 below outlines the functional blocks of the interface. The CODEC supports stereo playback and recording of audio signals at multiple sample rates with a resolution of 16-bit. The ADC and the DAC of the CODEC each contain two independent channels. Any ADC or DAC channel can be run at its own independent sample rate.

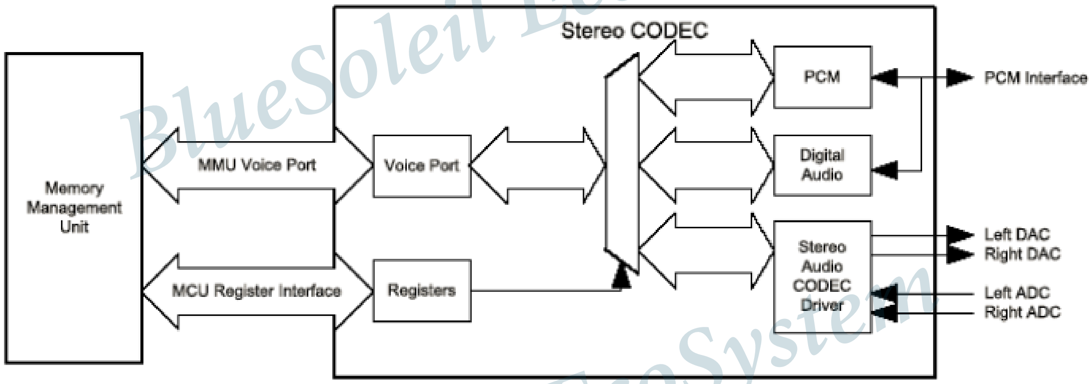

Figure 8 Audio Interface

The interface for the digital audio bus shares the same pins as the PCM CODEC interface, which means that each of the audio buses are mutually exclusive in their usage. These alternative functions are summarized in Figure 12 below.

Table 12 Alternative functions of the digital audio bus interface on the PCM interface

PCM Interface	SPDIF Interface	I2S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC		WS
PCM_CLK		SCK

6.1.1 Audio Input and Output

The audio input circuitry consists of a dual audio input that can be configured to be either single-ended or fully differential and programmed for either microphone or line input. It has an analogue and digital programmable gain stage for optimization of different microphones.

Audio signals are very sensitive to noise caused by the *Bluetooth* radio and it is highly recommended to always use fully differential signals.

The audio output circuitry consists of a dual differential class A-B output stage.

6.2 Stereo Audio CODEC Interface

The main features of the interface are as follows.

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for stereo digital audio bus standards such as I2S
- Support for IEC-60958 standard stereo digital audio bus standards, e.g. S/PDIF and AES3/EBU
- Support for PCM interfaces including PCM master CODECs that require an external system clock

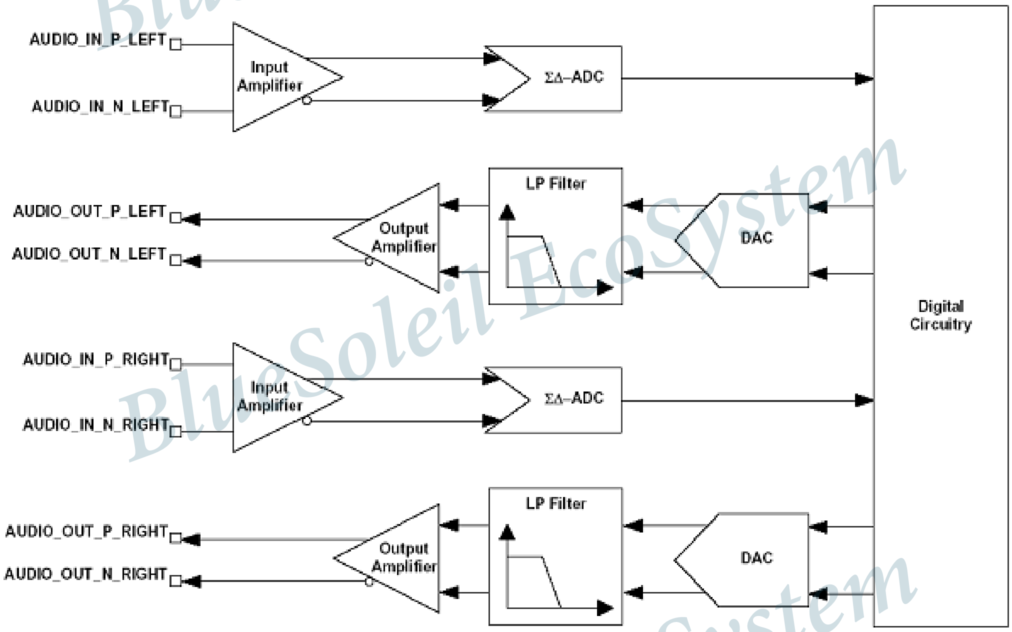

Figure 9 Stereo CODEC Audio Input and output Stages

The stereo audio CODEC uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a single power-supply of 1.5V and uses a minimum of external components.

6.2.1 ADC

The ADC consists of two second-order Sigma Delta converters allowing two separate channels that are identical in functionality, as shown in Figure 10.

Each ADC supports the following sample rates:

- 8kHz
- 11.025kHz
- 16kHz

- 22.05kHz
- 24kHz
- 32kHz
- 44.1kHz

The ADC contains two gain stages for each channel, an analogue and a digital gain stage. The digital gain stage has a programmable selection value in the range of 0 to 15 with the associated ADC gain settings summarized in Table 13 below. There is also a high resolution digital gain mode that allows the gain to be changed in 1/32dB steps. Please contact IVT Corporation for more information.

Table 13 ADC Digital Gain Rate Selection

Gain Selection Value	ADC Digital Gain Setting (dB)
0	0
1	3.5
2	6
3	9.5
4	12
5	15.5
6	18
7	21.5
8	-24
9	-20.5
10	-18
11	-14.5
12	-12
13	-8.5
14	-6
15	-2.5

The ADC analogue amplifier is a two-stage amplifier. The first stage of the analogue amplifier is responsible for selecting the correct gain for either microphone input or line input and, therefore, has two gain settings, one for the microphone and one for the line input. Refer to the chapter 6.2.4 and 6.2.5. In simple terms, the first stage amplifier has a selectable 24dB gain stage for the microphone and this creates the dual programmable gain required for the microphone or the line input. The equivalent block diagram for the two stages is shown in Figure 10 below.

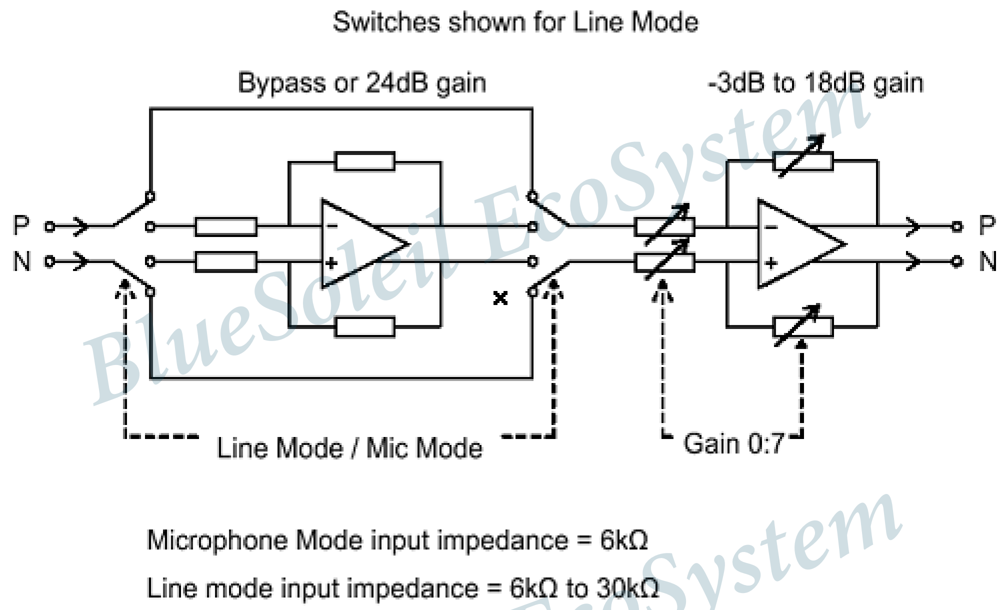

Figure 10 ADC Analogue Amplifier Block Diagram

The second stage of the analogue amplifier shown in Figure 10 has a programmable gain with seven individual 3dB steps. In simple terms, by combining the 24dB gain selection of the microphone input with the seven individual 3dB gain steps, the overall range of the analogue amplifier is approximately -3dB to 42dB in 3dB steps. The overall gain control of the ADC is controlled by a VM function.

6.2.2 DAC

The DAC consists of two third-order Sigma Delta converters allowing two separate channels that are identical in functionality as shown in Figure 10 above. Each DAC supports the following samples rates:

- 8kHz
- 11.025kHz
- 16kHz
- 22.050kHz
- 24kHz
- 32kHz
- 44.1kHz
- 48kHz

The default setting for A2DP is 44.1 kHz and for HFP 8 kHz.

The DAC contains two gain stages for each channel: a digital and an analogue gain stage. The digital gain stage has a programmable selection value in the range of 0 to 15 with associated DAC gain settings. This is summarized in Table 14. There is also a high resolution digital gain mode that allows the gain to be changed in 1/32dB steps. Please contact IVT Corporation for more information.

Table 14 DAC Digital Gain Rate Selection

Gain Selection Value	ADC Digital Gain Setting (dB)
0	0
1	3.5
2	6
3	9.5
4	12
5	15.5
6	18
7	21.5
8	-24
9	-20.5
10	-18
11	-14.5
12	-12
13	-8.5
14	-6
15	-2.5

The DAC analogue amplifier has a programmable gain with seven individual 3dB steps. The overall gain control of the DAC is controlled by a VM function. This setting is a combined function of the digital and analogue amplifier settings , therefore, for a 1V rms nominal digital output signal from the digital gain stage of the DAC, the following approximate output values of the analogue amplifier of the DAC can be expected:

Table 15 DAC Analogue Gain Rate Selection

Analogue Gain Setting	DAC Gain Setting (dB)
7	3
6	0
5	-3
4	-6
3	-9
2	-12
1	-15
0	-18

6.2.3 IEC 60958 Interface

The IEC 60958 interface is a digital audio interface that uses bi-phase coding to minimize the DC content of the transmitted signal and allows the receiver to decode the clock information from the transmitted signal. The IEC 60958 specification is based on the two industry standards AES/EBU and the Sony and Philips interface specification SPDIF. The interface is compatible with IEC 60958-1, IEC 60958-3 and IEC 60958-4.

The SPDIF interface signals are SPDIF_IN and SPDIF_OUT and are shared on the PCM interface pins. The input and output stages of the SPDIF pins can interface either to a 75Ω Coaxial cable with an RCA connector. See Figure 11 below. Or there is an option to use an optical link that uses Toslink optical components. See Figure 12 below.

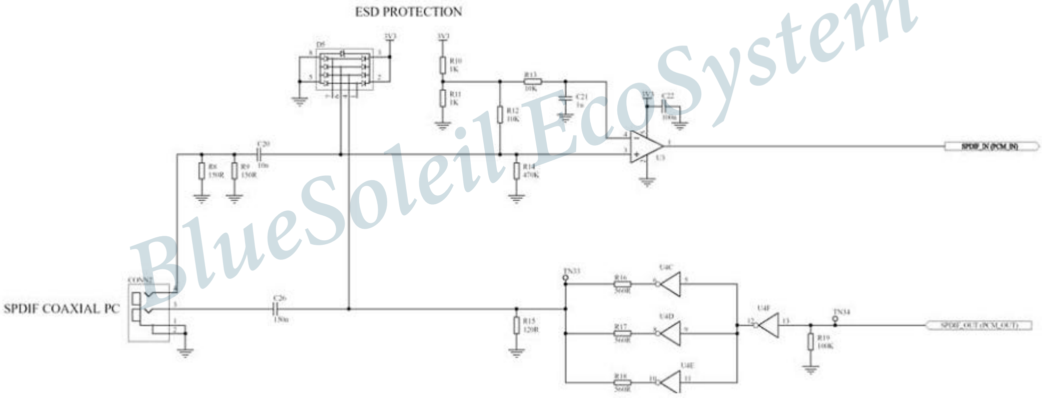

Figure 11 Example circuit for SPDIF interface (Co-Axial)

Figure 12 Example circuit for SPDIF interface (Optical)

6.2.4 Microphone Input

The audio-input is intended for use from 1μA@94dB SPL to about 10μA@94dB SPL. With biasing resistors R1 and R2 equal to 1kΩ, this requires microphones with sensitivity between about -40dBV and -60dBV.

The MIC_BIAS is like any voltage regulator and requires a minimum load to maintain regulation. The MIC_BIAS will maintain regulation within the limits 0.2~1.53 mA depending on the bias current setting. This means that if a microphone that sits below these limits is used, the microphone output must be pre-loaded with a large value resistor to ground.

MIC_BIAS line either is used as an enable signal for an external biasing regulator. The default setting for the bias current in i50e-A is 0.2 mA and it is recommended to use an external low noise biasing regulator for the best noise performance. The recommended microphone biasing circuitry is shown in Figure 13 below.

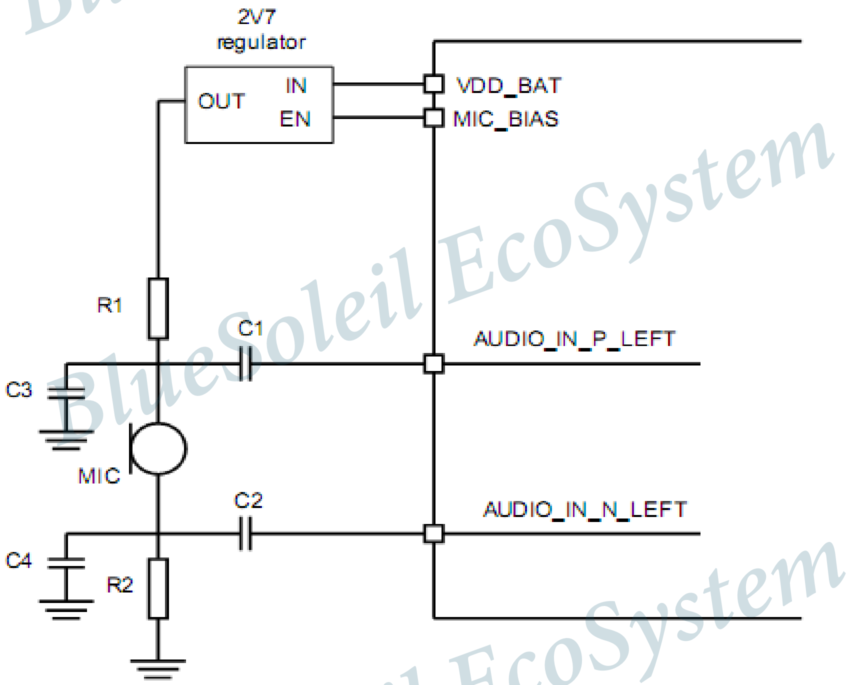

Figure 13 Recommended Microphone Biasing (left channel shown)

The input impedance at AUDIO_IN_N_LEFT, AUDIO_IN_P_LEFT, AUDIO_IN_N_RIGHT and AUDIO_IN_P_RIGHT is typically 6.0kΩ. C1 and C2 should be 150nF if bass roll-off is required to limit wind noise on the microphone. R1 sets the microphone load impedance and is normally in a range of 1 to 2kΩ. R2, C3 and C4 improve the supply rejection by decoupling supply noise from the microphone. Values should be selected as required. R1 may be connected to a convenient supply, in which case the bias network is permanently enabled, or to the output of the biasing regulator which may be configured to provide bias only when the microphone is required.

The microphone bias provides a 4-bit programmable output voltage with a 4-bit programmable output current, shown in Table 16 and Table 17.

Table 16 Voltage Output Step

Output Step	Typical Voltage Level (V)
0	1.71
1	1.76

2	1.82
3	1.87
4	1.95
5	2.02
6	2.10
7	2.18
8	2.32
9	2.43
10	2.56
11	2.69
12	2.9
13	3.08
14	3.33
15	3.57

Table 17 Current Output Step

Output Step	Typical Current (mA)
0	0.199
1	0.284
2	0.336
3	0.419
4	0.478
5	0.529
6	0.613
7	0.672
8	0.754
9	0.809
10	0.862
11	0.948
12	1.004
13	1.091
14	1.142
15	1.229

6.2.5 Line Input

If the input analogue gain is set to less than 21dB, i50e-A automatically selects line input mode. In line input mode, the first stage of the amplifier is automatically disabled, providing additional power saving. In line input mode, the input impedance varies from 6kΩ-30kΩ, depending on the volume setting. Figure 14 and Figure 15 show two circuits for line input operation and show connections for either differential or single-ended inputs.

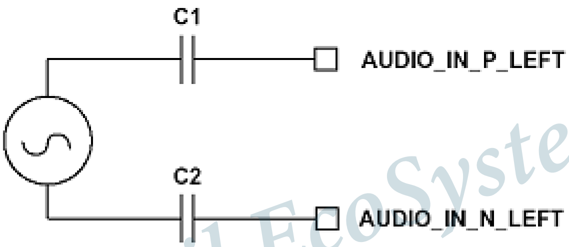

Figure 14 Differential input (left channel shown)

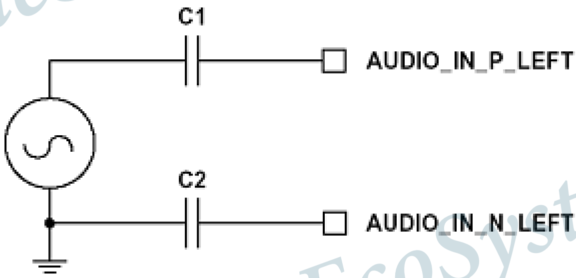

Figure 15 Single ended input (left channel shown)

6.2.6 Output Stage

The output digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to a 2Mbits/s 5-bit multi-bit bit stream, which is fed into the analogue output circuitry.

The output circuit is comprised of a digital to analogue converter with gain setting and an output amplifier. Its class AB output stage is capable of driving a signal on both channels of up to 2Vpk-pk differential into a load of 16Ω. The output is available as a differential signal between AUDIO_OUT_N_LEFT and AUDIO_OUT_P_LEFT for the left channel. See Figure 16 below; and between AUDIO_OUT_N_RIGHT and AUDIO_OUT_P_RIGHT for the right channel. The output is capable of driving a speaker directly if its impedance is at least 8Ω at reduced output swing and if only one channel is connected or an external regulator is used.

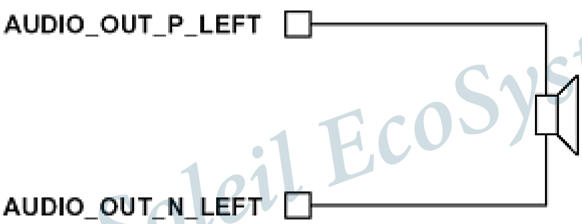

Figure 16 Speaker Output (left channel shown)

The analogue gain of the output stage is controlled by a 3-bit programmable resistive divider, which sets the gain in steps of approximately 3dB.

The multi-bit bit stream from the digital circuitry is low pass filtered by a third order filter with a pole at 20 kHz. The signal is then amplified in the fully differential output stage, which has a gain bandwidth of typically 1MHz.

6.2.6.1 Mono Operation

Mono operation is a single-channel operation of the stereo CODEC. The left channel represents the single mono channel for audio in and audio out. In mono operation, the right channel is an auxiliary mono channel that may be used in dual mono channel operation.

With single mono, the power consumption can be reduced by disabling the other channel.

6.2.6.2 Side Tone

In some applications, it is necessary to implement a side tone. This involves feeding an attenuated version of the microphone signal to the earpiece. The BlueCore5.Multimedia External CODEC contains a side tone circuitry to do this. The side tone hardware is configured through the following PS Keys:

PSKEY_SIDE_TONE_ENABLE

PSKEY_SIDE_TONE_GAIN

PSKEY_SIDE_TONE_AFTER_ADC

PSKEY_SIDE_TONE_AFTER_DAC

6.2.6.3 Integrated Digital Filter

TBA

6.3 Digital Audio Interface (I2S)

The digital audio interface supports the industry standard formats for I2S, left-justified (LJ) or right-justified (RJ). The interface shares the same pins as the PCM interface, which means that each audio bus is mutually exclusive in its usage. These alternative functions are summarized in Table 18 below. Figure 17 shows the timing diagram.

Table 18 Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

PCM Interface	I2S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

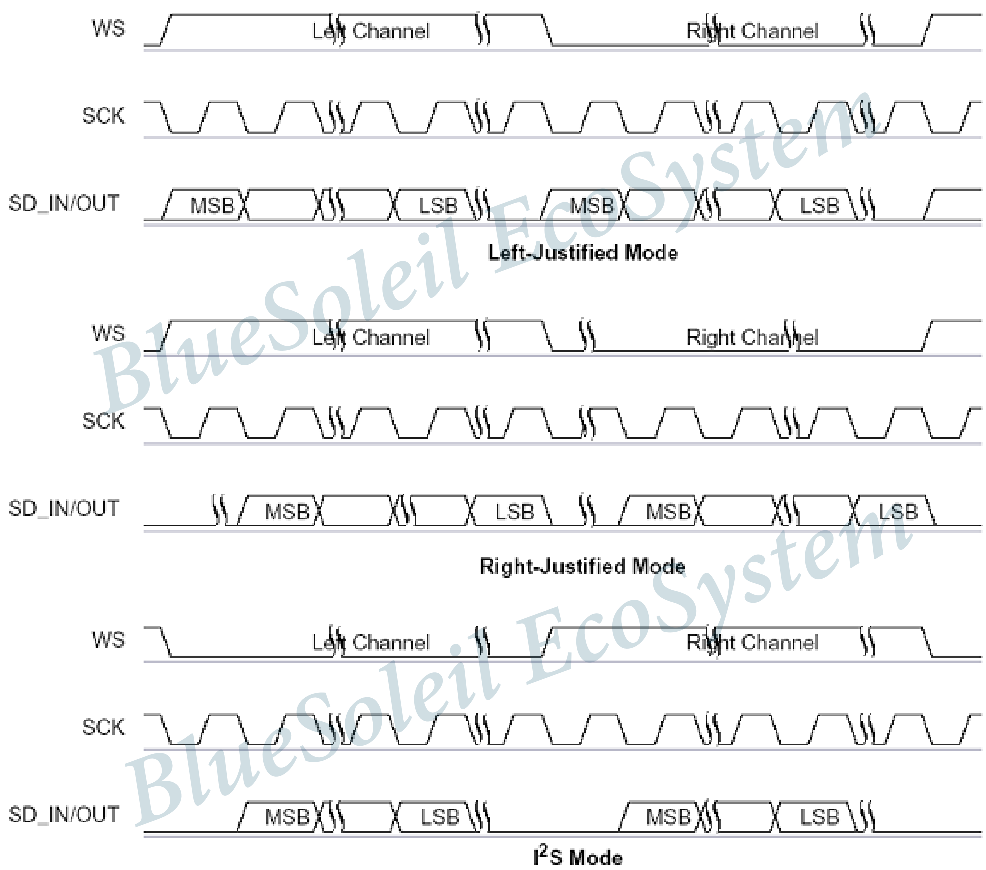

Figure 17 Digital Audio Interface Modes

Table 19 below introduces the values for the PS Key (PSKEY_DIGITAL_AUDIO_CONFIG) that is used to set-up the digital audio interface. For example, to configure an I2S interface with 16-bit SD data set PSKEY_DIGITAL_CONFIG to 0x0406.

Table 19 PSKEY_DIGITAL_AUDIO_CONFIG

Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0 for left justified, 1 for right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: 0 is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period.
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	For 0, SD data is left channel when WS is high. For 1 SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	For 0, 17 bit SD data is rounded down to 16 bits. For 1, the audio attenuation defined

			in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00F0	CONFIG_AUDIO_ATTE	Attenuation in 6 dB steps.
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN, 00=16 bit, 01=20 bit, 10=24 bit, 11=Reserved. This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	For 0, 17 bit SD_IN data is rounded down to 16 bits. For 1 only the most significant 16 bits of data are received.

The internal representation of audio samples withinBlueCore5.Multimedia External is 16-bit and data on SD_OUT is limited to 16-bit per channel. Digital audio interface slave timing refers to Table 20 and Figure 18 below.

Table 20 Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHZ
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{ssu}	WS to SCK set-up time	20	-	-	ns
t_{sh}	WS to SCK hold time	20	-	--	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hole time	20	-	-	ns

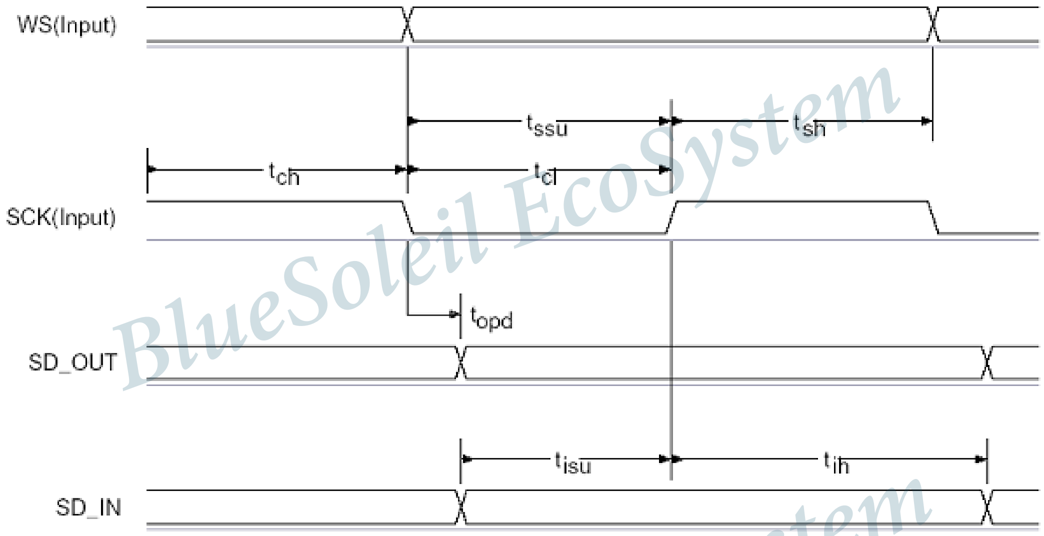

Figure 18 Digital Audio Interface Slave Timing

Digital audio interface slave timing refers to Table 21 and Figure 19 below.

Table 21 Digital Audio Interface Master Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHZ
-	WS Frequency	-	-	96	kHz
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{spd}	SCK to WS delay	-	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hole time	20	-	-	ns

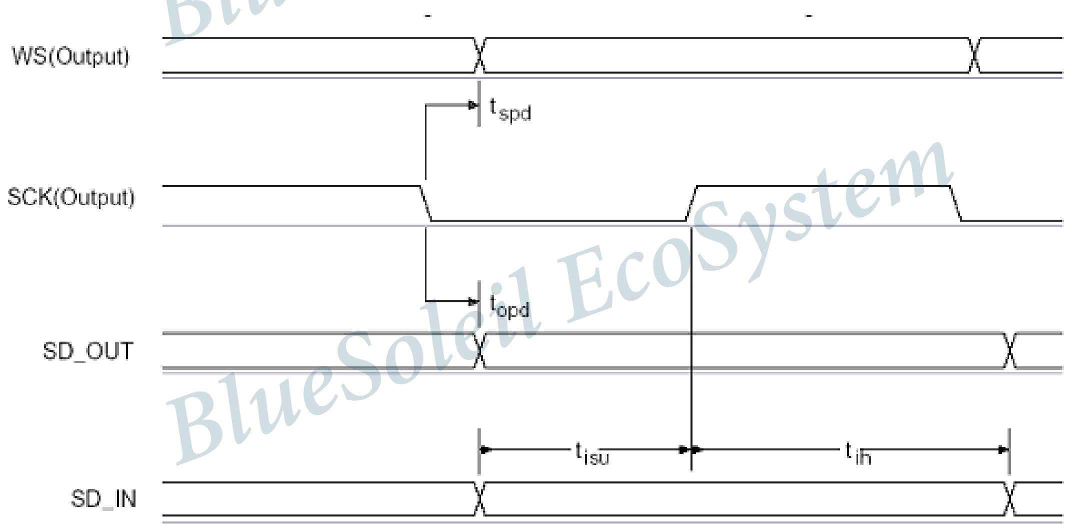

Figure 19 Digital Audio Interface Master Timing

6.4 PCM Interface

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, i50e-A has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. i50e-A offers a bi directional digital audio interface that routes directly into the baseband layer of the on chip firmware. It does not pass through the HCI protocol layer.

Hardware on i50e-A allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any one time.

i50e-A can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz.When configured as PCM interface slave it can operate with an input clock up to 2048kHz. i50e-A is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit µ-law or A-law companded sample formats at 8k samples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS _KEY_PCM_CONFIG32 (0x1b3). i50e-A interfaces directly to PCM audio devices are follows:

Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices

OKI MSM7705 four channels A-law and µ-law CODEC

Motorola MC145481 8-bit A-law and µ-law CODEC

Motorola MC145483 13-bit linear CODEC

STW 5093 and 5094 14-bit linear CODECs

BlueCore4-External is also compatible with the Motorola SSI™ interface

6.4.1 PCM Interface Master/Slave

When configured as the Master of the PCM interface, i50e-A generates PCM_CLK and PCM_SYNC. See Figure 20 below.

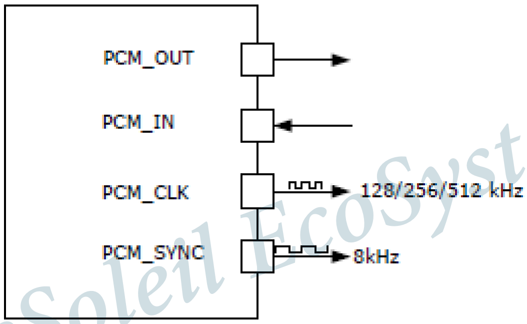

Figure 20 i50e-A as PCM Master

When configured as the Slave of the PCM interface, i50e-A accepts PCM_CLK and PCM_SYNC. PCM_CLK rates up to 2048kHz are accepted. See Figure 21 below.

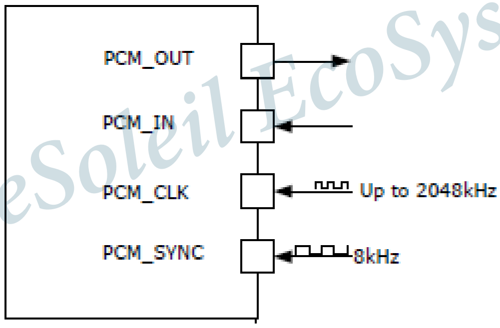

Figure 21 i50e-A as PCM slave

6.4.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When i50e-A is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore5 MM is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e. 62.5µs long.

i50e-A samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge. See Figure 22 below.

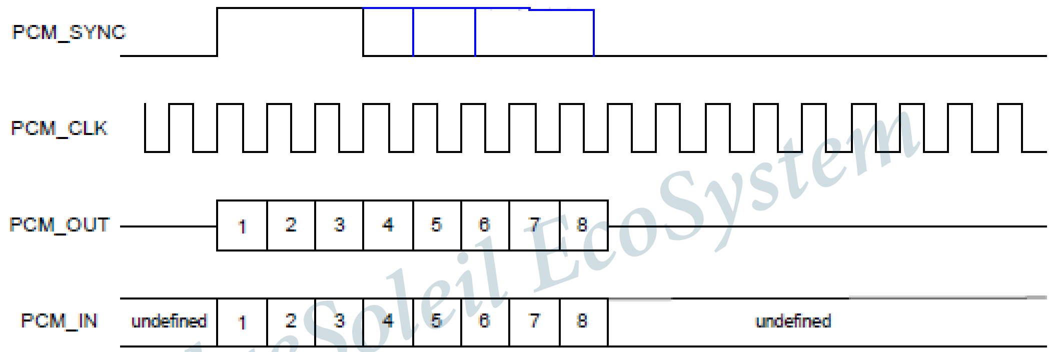

Figure 22 Long Frame Sync (shown with 8-bit Companded Sample)

6.4.3 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long. See Figure 23 below.

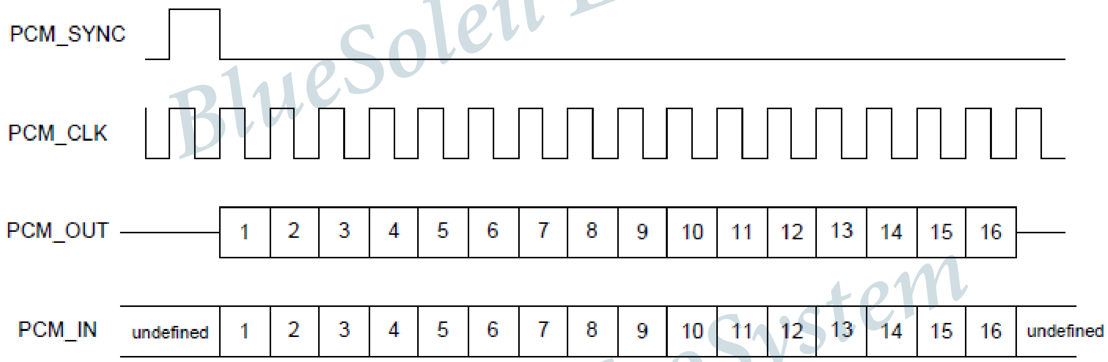

Figure 23 Short Frame Sync (shown with 16-bit Companded Sample)

As with Long Frame Sync, i50e-A samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

6.4.4 Multi Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots. See Figure 24 below.

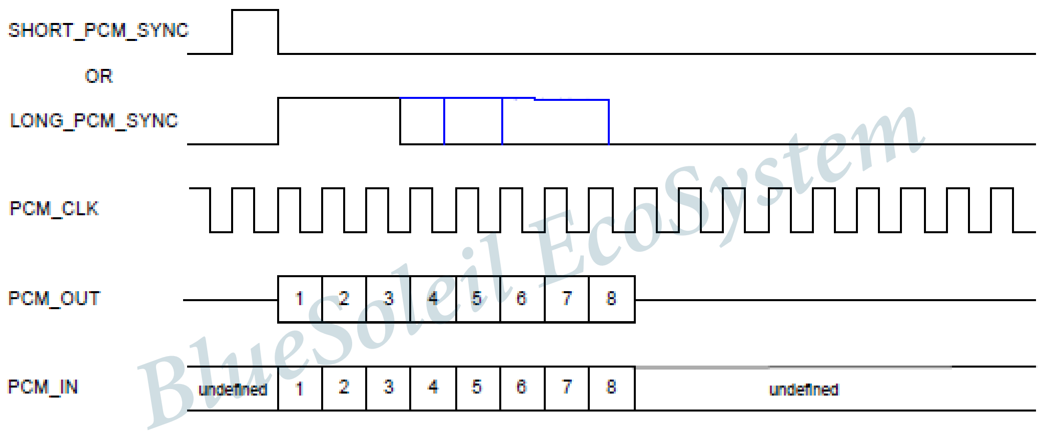

Figure 24 Multi Slot Operation with Two Slots and 8-bit Companded Samples

6.4.5 GCI Interface

i50e-A is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured. See Figure 25 below.

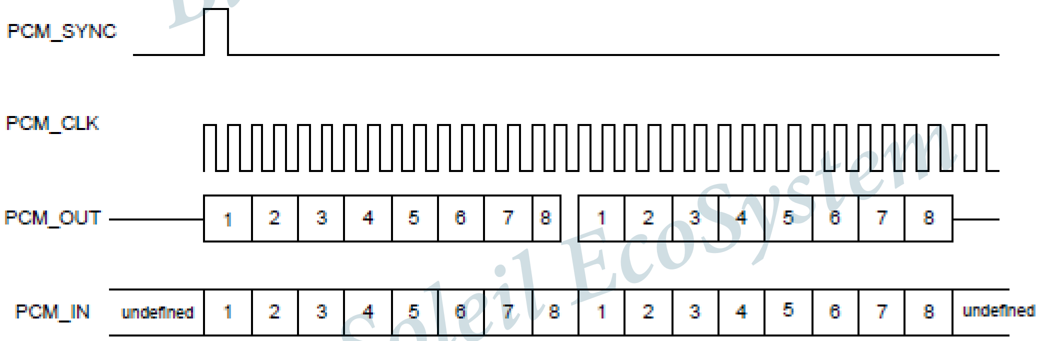

Figure 25 GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With i50e-A in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

6.4.6 Slots and Sample Formats

i50e-A can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Duration's of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8, 13 or 16-bit sample formats.

i50e-A supports 13-bit linear, 16-bit linear and 8-bit µ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big Endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs. See Figure 26 below.

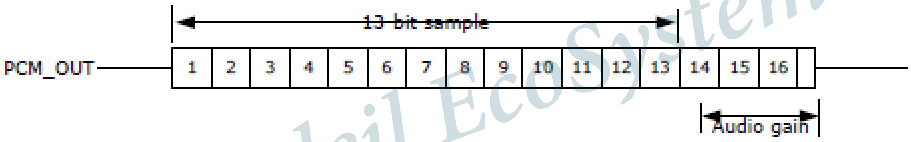

Figure 26 16-bit Slot with 13-bit Linear Sample and Audio Gain Selected

6.4.7 Additional Features

i50e-A has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

6.4.8 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. They are summarized in Table 22 and Table 23 below. The default for PSKEY_PCM_CONFIG32 key is 0x00800000 i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-stating of PCM_OUT.

Table 22 PSKEY_PCM_CONFIG32

Name	Bit position	Description
-	0	Set to 0
SLAVE MODE EN	1	0 selects Master mode with internal generation of PCM_CLK and PCM_SYNC. 1 selects Slave mode requiring externally generated PCM_CLK and PCM_SYNC. This should be set to 1 if 48M_PCM_CLK_GEN_EN (bit 11) is set.
SHORT SYNC EN	2	0 selects long frame sync (rising edge indicates start of frame), 1 selects short frame sync (falling edge indicates start of frame).
-	3	Set to 0
SIGN EXTENDED EN	4	0 selects padding of 8 or 13-bit voice sample into a 16- bit slot by inserting extra LSBs, 1 selects sign extension. When padding is selected with 3-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit samples the 8 padding bits are zeroes.
LSB FIRST EN	5	0 transmits and receives voice samples MSB first, 1 uses LSB

		first.
TX TRISTATE EN	6	0 drives PCM_OUT continuously, 1 tri-states PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX TRISTATE RISING EDGE EN	7	0 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is also not active. 1 tristates PCM_OUT after the rising edge of PCM_CLK.
SYNC SUPPRESS EN	8	0 enables PCM_SYNC output when master, 1 suppresses PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilize this to enter a low power state.
GCI MODE EN	9	1 enables GCI mode.
MUTE EN	10	1 forces PCM_OUT to 0.
48M PCM CLK GEN EN	11	0 sets PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock, as for BlueCore4-External. 1 sets PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG LENGTH SYNC EN	12	0 sets PCM_SYNC length to 8 PCM_CLK cycles and 1 sets length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER CLK RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE SLOT	[26:23]	Default is 0001. Ignored by firmware
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration 8 (0b11) bit sample 8 cycle slot duration.

Table 23 PSKEY_PCM_LOW_JITTER_CONFIG

Name	Bit position	Description
CNT LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT RATE	[23:16]	Sets PCM_CLK count rate.
SYNC LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK.

7 Software Stacks

BlueSoleil i50e-A is supplied with *Bluetooth* v3.0+EDR compliant stack firmware, which runs on the internal RISC microcontroller. The i50e-A software architecture allows *Bluetooth* processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any).

7.1 BlueSoleil Stack

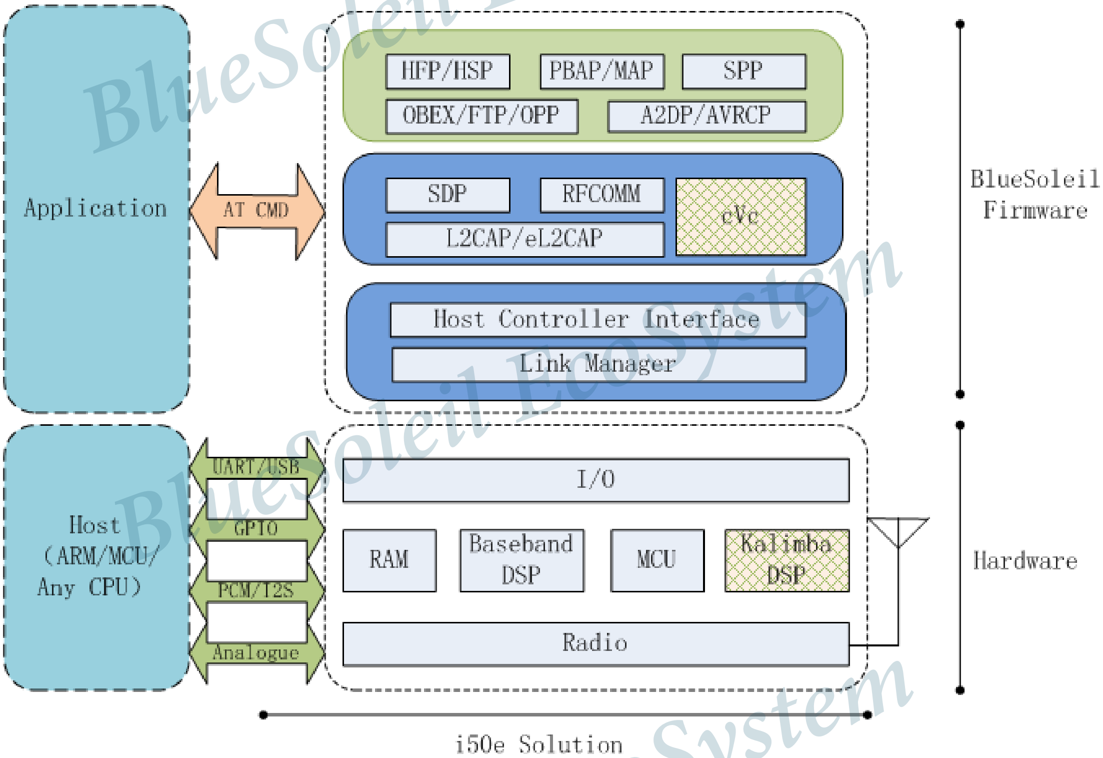

Figure 27 BlueSoleil Stack

As illustrated in Figure 27 above, no host processor is required to run the *Bluetooth* protocol stack. All BlueSoleil stack layers, including application software, run on the internal RISC processor.

The host processor interfaces to BlueSoleil stack of i50e-A via one or more of the physical interfaces, which are also shown in the figure 27. The most common interfacing is done via UART interface using the ASCII commands supported by the BlueSoleil stack. With these ASCII commands the user can access *Bluetooth* functionality without paying any attention to the complexity, which lies in the *Bluetooth* protocol stack.

The user may write applications code to run on the host processor to control BlueSoleil stack with ASCII commands and to develop *Bluetooth* powered applications. Please refer to BlueSoleil_I50e_Programming_Manual.pdf.

8 Enhanced Data Rate

EDR has been introduced to provide 2x and optionally 3x data rates with minimal disruption to higher layers of the Bluetooth stack. CSR supports both of the new data rates, with i50e-A.

8.1 Enhanced Data Rate Baseband

At the baseband level EDR uses the same 1.6kHz slot rate as basic data rate and therefore the packets can be 1, 3, or 5 slots long as per the basic data rate. Where EDR differs from the basic data rate is that in the same 1MHz symbol rate 2 or 3bits are used per symbol, compared to 1bit per symbol used by the basic data rate. To achieve the increase in number of bits symbol, two new modulation schemes have been introduced as summarized in Table 24 presented below and the modulation schemes are explained in the further sections.

Table 24 Data Rate Schemes

Scheme	Bits per symbol	Modulation
Basic data rate	1	GFSK
Enhanced data rate	2	P/4 DQPSK
Enhanced data rate	3	8DPSK (optional)

Although the EDR uses new packets Link establishment and management are unchanged and still use Basic Rate packets.

8.2 Enhanced Data Rate _/4 DQPSK

4 DQPSK includes the following features.

- 4-state Differential Phase Shift Keying.
- 2 bits determine phase shift between consecutive symbols. See Table 25 below.
- S/4 rotation avoids phase shift of S, which would cause large amplitude variation.
- Raised Cosine pulse shaping filter to further reduce side band emissions.

Table 25 2 bits Determine Phase Shift Between Consecutive Symbols

Bit pattern	Phase shift
00	Π/4
01	3 Π/4
10	–3 Π/4
11	– Π/4

8.3 8DQPSK

8DQPSK includes the following features.

- 8-state Differential Phase-Shift Keying. See Figure 28 below.
- Three bits determine phase shift between consecutive symbols. See Table 26 below.

Table 26 3 bits Determine Phase Shift between Consecutive Symbols

Bit pattern	Phase shift
000	0
001	Π/4
011	Π/2
010	3 Π/4
110	Π
111	−3 Π/4
101	− Π/2
100	− Π/4

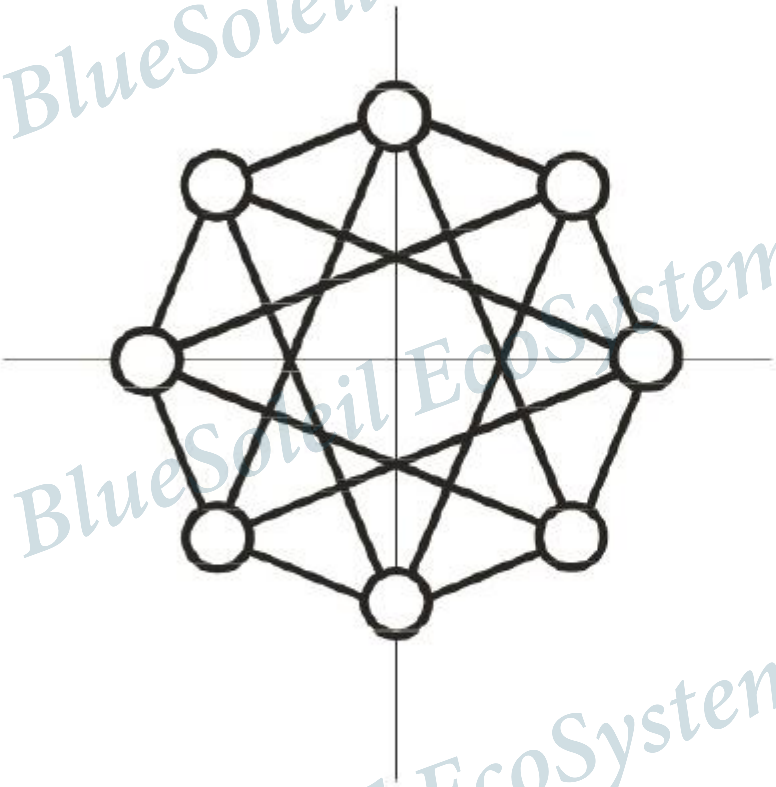

Figure 28 8DQPSK

9 Re-flow Temperature-time Profile

The re-flow profiles are illustrated in Figure 29 and Figure 30 below.

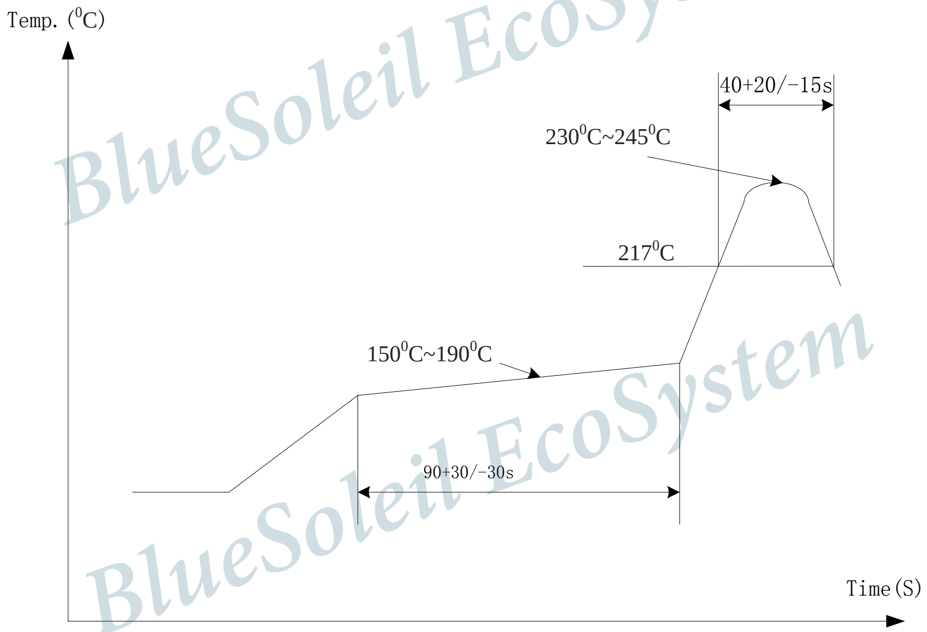

Figure 29 Typical Lead-Free Re-flow Solder Profile

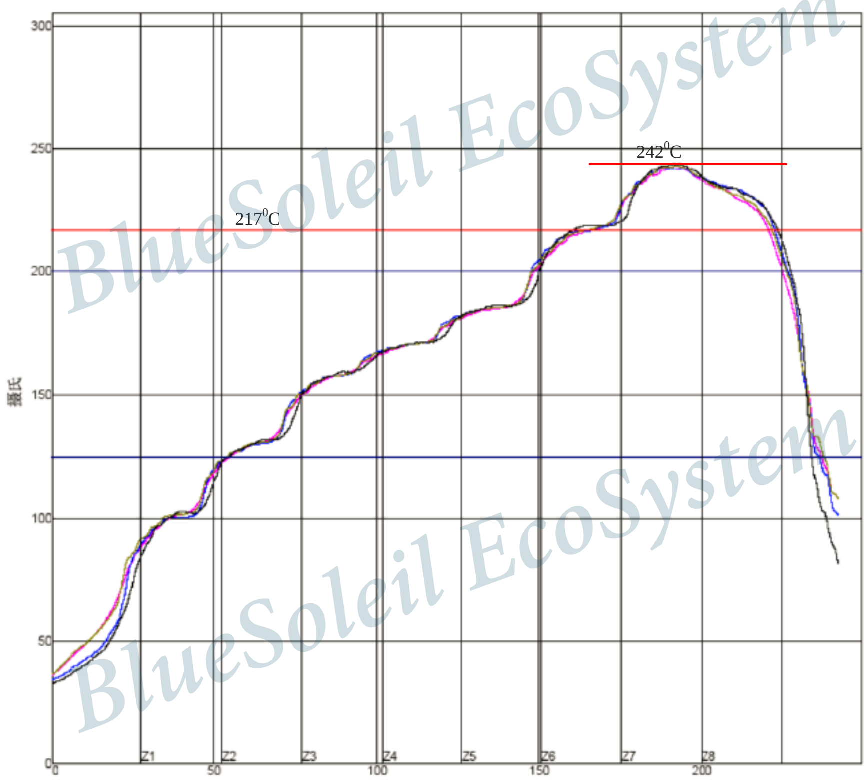

Figure 30 Typical Lead-free Re-flow

The soldering profile depends on various parameters according to the use of different solder and material. The data here is given only for guidance on solder re-flow. i50e-A will withstand up to two re-flows to a maximum temperature of 245°C.

10 Reliability and Environmental Specification

10.1 Temperature Test

Put the module in demo board which uses exit power supply, power on the module and connect to mobile. Then put the demo in the -40℃ space for 1 hour and then move to +85℃ space within 1minute, after 1 hour move back to -40℃ space within 1 minute. This is 1 cycle. The cycles are 32 times and the units have to pass the testing.

10.2 Vibration Test

The module is being tested without package. The displacement requests 1.5mm and sample is vibrated in three directions(X,Y,Z). Vibration frequency set as 0.5G, a sweep rate of 0.1 octave/min from 5Hz to 100Hz last for 90 minutes each direction. Vibration frequency set as 1.5G, a sweep rate of 0.25 octave/min from 100Hz to 500Hz last for 20 minutes each direction.

10.3 Desquamation Test

Use clamp to fix the module, measure the pull of the component in the module, make sure the module`s soldering is good.

10.4 Drop Test

Free fall the module (condition built in a wrapper which can defend ESD) from 150cm height to cement ground, each side twice, total twelve times. The appearance will not be damaged and all functions OK.

10.5 Packaging Information

After unpacking, the module should be stored in environment as follows.

- Temperature: 25℃ ±2℃

- Humidity: <60%
- No acidity, sulfur or chlorine environment

The module must be used in four days after unpacking.

11 Layout and Soldering Considerations

11.1 Enhanced Data Rate Baseband

i50e-A is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used.

IVT Corporation will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

- Avoid using more than one flow.
- Reliability of the solder joint and self-alignment of the component are dependent on the solder volume. Minimum of 150um stencil thickness is recommended.
- Aperture size of the stencil should be 1:1 with the pad size.

A low residue, “no clean” solder paste should be used due to low mounted height of the component

11.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding via separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND via all around the PCB edges.

Restricted Area

The mother board should have no bare conductors or via in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or via) are allowed in this area, because of mismatching the on-board antenna.

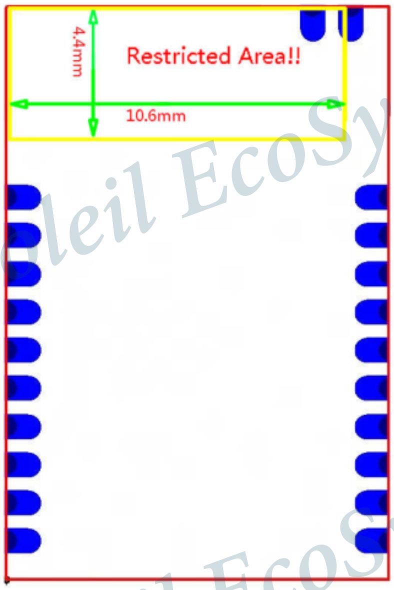

Figure 31 i50e-A Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground via around it. Locate them tightly and symmetrically around the signal via. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

Audio Layout

Route audio lines as differential pairs. The positive and negative signals should run parallel and close to each other until they are converted to single-ended signals. Use dedicated audio ground plane for entire audio section.

12 Physical Dimensions

BlueSoleil i50e-A's dimension is 23.9mm(L)x15.9mm(W).

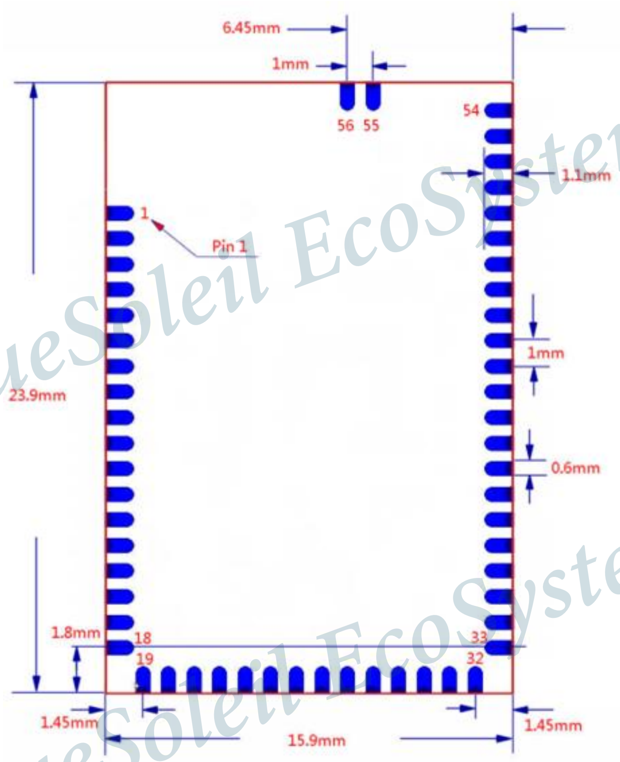

Figure 32 i50e-A Footprint

13 Package

TBD.

14 Certifications

BlueSoleil i50e-A is compliant to the following specifications.

14.1 Bluetooth

BlueSoleil i50e module is qualified as a *Bluetooth* controller subsystem and it fulfills all the mandatory requirements of *Bluetooth* 3.0 + EDR core specification. If not modified in any way, it is a complete *Bluetooth* entity, containing software and hardware functionality as well as the whole RF-part excluding the antenna. This practically translates to that if the module is used without modification of any kind, it does not need any *Bluetooth* approval work for evaluation on what needs to be tested.

i50e Qualified Design ID (QDID): B017206

i50e qualified listing details:

https://www.bluetooth.org/tpg/QLI_viewQDL.cfm?qid=17206

i50e PICS details:

https://www.bluetooth.org/tpg/showCorePICS.cfm?3A000A5A005C5043535E5214403B0C0D0E2405022413010E57503F202A5A705A564050

i50e End Product Detail:

https://www.bluetooth.org/tpg/EPL_Detail.cfm?ProductID=15034

14.2 CE 0700

Hereby, IVT Corporation declares that this device is in compliance with the essential requirements and other relevant provisions of Directive 1999/5/EC.

CE 0700

14.3 FCC

FCC IDENTIFIER:	S78-IVTI50E
Name of Grantee:	IVT Corporation
Equipment Class:	**Part 15 Spread Spectrum Transmitter**
Notes:	**Bluetooth Module**
Modular Type:	**Limited Single Modular**

14.4 IC

CERTIFICATION NUMBER: IC: 11004A-IVTI50E

Issued to/Délivré a: IVT Corporation **Date Issued:** 7/8/2013
Address: 5/F, Zhongguancun Fazhan Building No. 12, Shangdi Xinxi Road, Haidian District, Beijing

Nature of Application/Nature d'Application:	Original
Equipment Description/Genre de Matériel:	Bluetooth module
Type of Radio Equipment:	Limited Modular Approval, Low Power Device (2400-2483.5 MHz)
Equipment Category/Catégorie de Matériel:	Category I
Model Number(s)/Modele	i50e

15 RoHS Statement with a List of Banned Materials

i50e meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

The following banned substances are not present in i50e, which is compliant with RoHS:

- Cadmium
- Lead
- Mercury
- Hexavalent chromium
- PBB (Polybrominated Bi-Phenyl)
- PBDE (PolybrominatedDiphenyl Ether)

16 *Bluetooth* Technology Best Developed Corporation

IVT Corporation is one of *Bluetooth* technology BEST developed together which is authenticated by The Bluetooth SIG. See Figure 33 below.

Figure 33 IVT is One of *Bluetooth* Technology BEST Developed Together

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